

WHAT IS CLAIMED IS:

1. A method for reducing the possibility of cold reset in a computer system that includes a central processing unit (CPU), a wake-up button that is used to awaken the CPU from a sleep mode, and a battery that supplies power to the computer system, the CPU supporting the function of software battery fault handling, and the method comprising :

when the CPU is in the sleep mode and the computer system's power supply is in an uncertain status, the CPU staying in the sleep mode even a wake-up event occurs; and

when the CPU is in the sleep mode and the period during which the wake-up button is pressed is less than a predetermined value, the CPU continues to stay in the sleep mode.

2. The method according to claim 1, wherein the uncertain power supply status is the status of battery fault.

3. The method according to claim 1, wherein the uncertain power supply status is the status when the battery lid is opened.

4. The method according to claim 1, wherein the uncertain power supply status is the status when the battery is in low power.

5. The method according to claim 1, wherein the computer system is a personal digital assistant (PDA).

6. The method according to claim 1, wherein the predetermined value is greater than the general value of the period during which the wake-up button is pressed due to a collision or an impact, and less than the general value of the period during which the user intentionally presses the wake-up button.

5 7. The method according to claim 1, wherein the predetermined value is greater than 1~2 millisecond and is less than 100 millisecond.

8. A computer system comprising:

a CPU that is used to control the computer system, and the CPU supports the function of software battery fault handling;

10 a circuit unit that is electrically connected to the CPU, and is used to receive a wake-up event and to selectively output the wake-up event to the CPU;

a detection circuit that is used to control the circuit unit according to the status of the computer system; and

15 a battery that supplies power to the computer system;

wherein when the CPU is in the sleep mode and the detection circuit has detected that the computer system is in a status of uncertain power supply, the CPU is still kept in the sleep mode even though the wake-up event has been sent to the circuit unit.

20 9. The computer system according to claim 8, wherein the uncertain power supply status is the status of battery fault.

10. The computer system according to claim 8, wherein the uncertain power supply status is the status when the battery lid is opened.

11. The computer system according to claim 8, wherein the uncertain power supply status is the status when the battery is in low power.

5 12. The computer system according to claim 8, wherein the computer is a personal digital assistant (PDA).

13. A computer system comprising:

a wake-up button;

a CPU that is used to control the computer system and the CPU

10 supports the function of software battery fault handling; and

a delay protection circuit that is used to detect the status of the wake-up button;

wherein when the computer system is in the sleep mode and the delay protection circuit has detected that the period during which the wake-up

15 button is pressed is less than a predetermined value, then the CPU continues to stay in the sleep mode.

14. The computer system according to claim 13, wherein when the computer system is in the sleep mode, the delay protection circuit is enabled; when the computer system is in normal operation mode, the delay protection
20 circuit is disabled.

15. The computer system according to claim 13, wherein the

predetermined value is greater then the general value of the period during which the wake-up button is pressed because of a collision or an impact, and is less then the general value of the period during which the user intentionally presses the wake-up button.

5 16. The computer system according to claim 13, wherein the computer system is a personal digital assistant (PDA).

17. The computer system according to claim 13, wherein the predetermined value is greater than 1~2 millisecond, and is less than 100 millisecond.

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